We claim:

1. A method for making a programmable resistance memory element, comprising:

providing a conductive material;

forming a sidewall spacer over said conductive material;

using said sidewall spacer as a mask, removing a portion of said conductive material to form a raised portion of said conductive material under said spacer; and

forming a programmable resistance material in electrical contact with said raised portion.

2. The method of claim 1, wherein said removing step comprises etching said conductive material.

3. The method of claim 2, wherein said etching step comprises anisotropically etching said conductive material.

4. The method of claim 2, wherein said etching step comprises isotropically etching said conductive material.

5. The method of claim 1, wherein said forming said sidewall spacer step comprises:

forming a second layer over said conductive material;

forming a sidewall surface in said second layer;

forming a third layer over said sidewall surface; and

removing a portion of said third layer.

6. The method of claim 5, further comprising:

forming a first layer over said conductive material and then forming said second layer over said first layer.

7. The method of claim 6, further comprising:

after removing said portion of said third layer, removing said second layer; and

removing a portion of said first layer.

8. The method of claim 5, wherein said removing said portion of said third layer step comprises anisotropically etching said third layer.

9. The method of claim 6, wherein said removing said portion of said first layer comprises anisotropically etching said first layer.

10. The method of claim 6, wherein said first and third layers are oxides.

11. The method of claim 5, wherein said second layer is polysilicon.

12. The method of claim 6, wherein said first and third layers are nitrides.

13. The method of claim 5, wherein said second layer is an oxide.

14. The method of claim 1, wherein said sidewall spacer comprises a material selected from the group consisting of dielectric, semiconductor, and conductor.

15. The method of claim 1, wherein said sidewall spacer comprises a material selected from the group consisting of oxide and nitride.

16. The method of claim 1, wherein said sidewall spacer comprises polysilicon.

17. The method of claim 1, wherein said programmable resistance material comprises a phase change material.

18. The method of claim 1, wherein said programmable resistance material comprises a chalcogen element.